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W&B-INF-1850

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By: Hongtang Chen Date: March 27, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No. : 10/613,367 Confirmation No. 4886
Applicant : Carsten Ohlhoff et al.
Filed : July 3, 2003
TC/A.U. : 2138
Examiner : Cynthia Britt
Title : Test Circuit and Method for Testing an
Integrated Memory Circuit

Docket No. : W&B-INF-1850
Customer No. : 24131

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

S i r :

In response to the Office action dated January 24, 2006,
please consider the following:

Remarks/Arguments begin on page 5 of this paper.